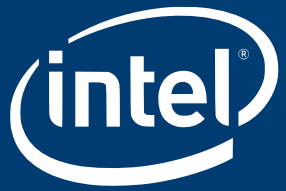

# SP FP TANGENT ARCHITECTURE FOR FPGAS

Bogdan Pasca, Martin Langhammer
Intel PSG

Arithmetic in DSP (Special Session), Tuesday, July 25th, 2017

# This talk is about

- single-precision tangent implementation
- input range restricted to $[-\pi/2, \pi/2]$
- accuracy can be tunned to meet OpenCL conformance
- target contemporary FPGAs having hard FP DSPs
- available in DSP Builder Advanced backend

- this work builds on
  Faithful Single-Precision Floating-Point Tangent for FPGAs
  Field Programmable Gate Arrays 2013 (FPGA'13)

# Context

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  - efficient for iterative implementations
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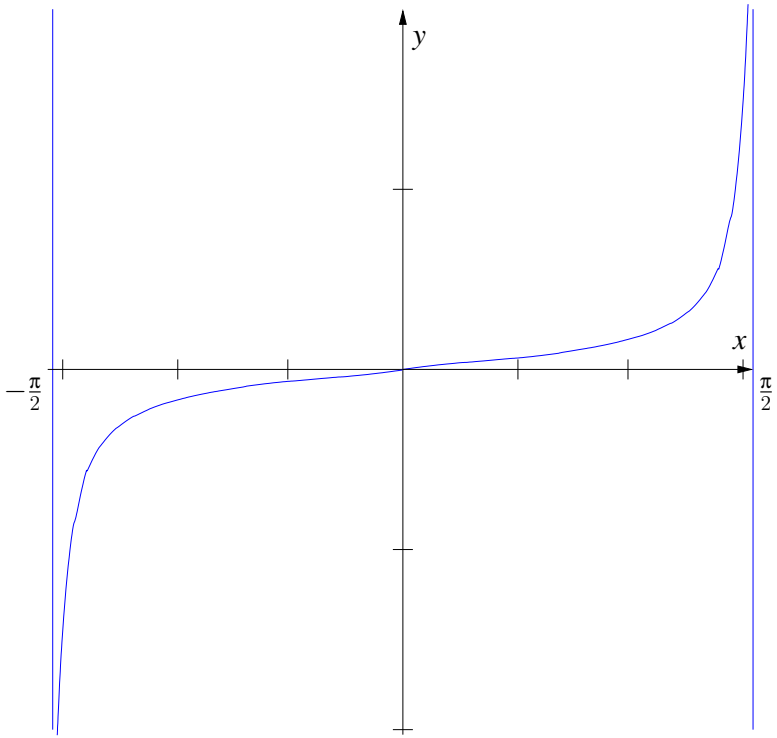
- piecewise polynomial-approximation can also be used [6]
  - better mapping to FPGA architecture
  - can use operator assembly, but that can be wasteful [1, 5]
- implementation as a fused-operator
  - careful error analysis
  - can obtain faithfully rounded SP tangent

# Technique

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- range-reduction step not presented here [2, 7]

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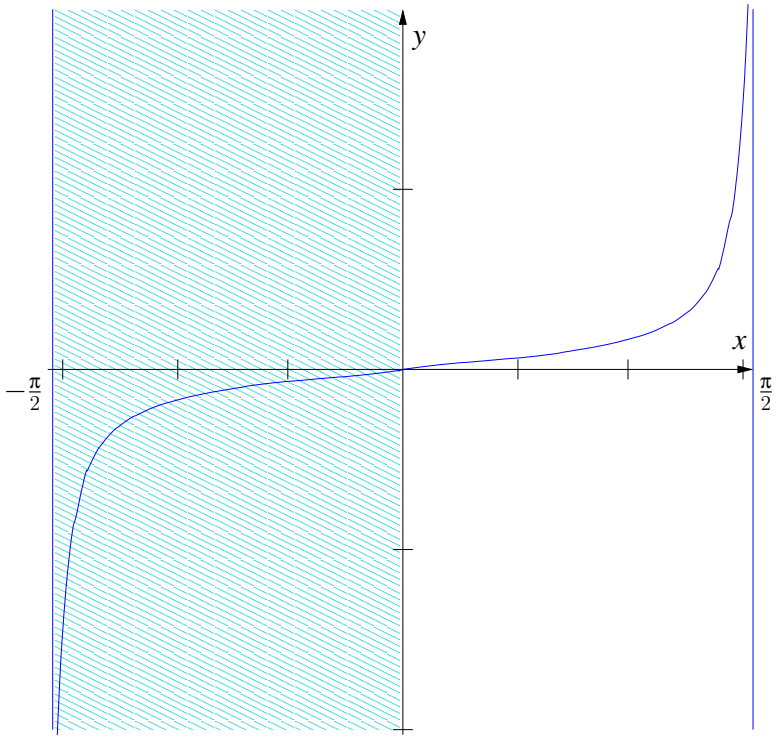


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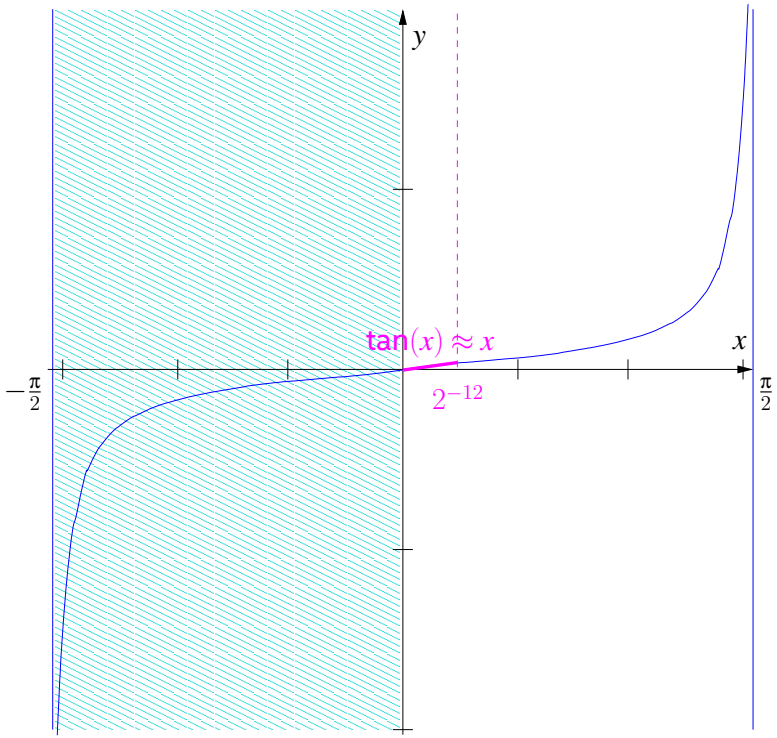


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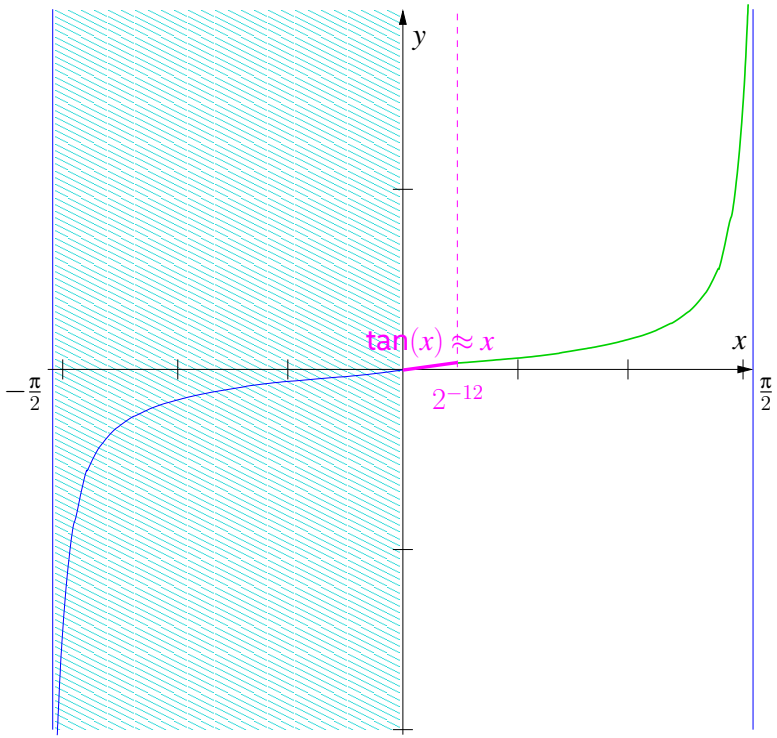


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- 24+12=36 bit fixed-point for compute range input

# Technique

- the following identity holds:

$$\tan(a+b) = \frac{\tan(a)+\tan(b)}{1-\tan(a)\tan(b)}$$

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$$\tan(a+b) = \frac{\tan(a)+\tan(b)}{1-\tan(a)\tan(b)}$$

- this can be expanded recursively to:

$$\tan(a+b+c) = \frac{\frac{\tan(a)+\tan(b)}{1-\tan(a)\tan(b)}+\tan(c)}{1-\frac{\tan(a)+\tan(b)}{1-\tan(a)\tan(b)}\tan(c)}$$

- decompose input as: $x = c+a+b$
  - weight of the MSB of $c$ is $2^0$

$x$

| c | a | b |
|---|---|---|
| 9 bits | 9 bits | 18 bits |

# Approximating the numerator

$$n = \frac{\tan(a) + \tan(b)}{1 - \tan(a)\tan(b)} + \tan(c)$$

- $\tan(b) \in [0, 2^{-17}]$, $\tan(a) \in [0, 2^{-8}]$
- $\tan(a)\tan(b) \in [0, 2^{-25}] \rightarrow 1 - \tan(a)\tan(b) \approx 1$

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- numerator approximated by:

$$n = \tan(a) + b + \tan(c)$$

# Approximating the denominator

$$d = 1 - \frac{\tan(a) + \tan(b)}{1 - \tan(a)\tan(b)} \tan(c)$$

- use the same technique $1 - \tan(a)\tan(b) \approx 1$, $\tan(b) \approx b$
- possible cancellation can amplify an existing error
- cancellation occurs $x$ close to $\pi/2$
- use additional table for the final 512ulp before $\pi/2$

- denominator approximated by:

$$d = 1 - (\tan(a) + b)\tan(c)$$

# Implementation using Hard FP DSP Blocks

- Alignment:
  - $c$ and $a$ are obtained from $x_{fxp}$
  - reduced barrel shifter size: use top 18 bits of the $M_x$
  - maximum shift size is 13 ($tan(x) = x$ if required shift $> 13$)

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- B in floating-point:
  - use mask to extract FP information

| $e$ | $e_{biased}$ | mask |
|---|---|---|
| 0 | 01111111 | 00000000000000000111111 |
| -1 | 01111110 | 00000000000000001111111 |
| -2 | 01111101 | 00000000000000011111111 |
| -3 | 01111100 | 00000000000000111111111 |
| -4 | 01111011 | 00000000000001111111111 |
| -5 | 01111010 | 00000000000011111111111 |
| -6 | 01111001 | 00000000000111111111111 |
| -7 | 01111000 | 00000000001111111111111 |
| -8 | 01110111 | 00000000011111111111111 |
| -9 | 01110110 | 00000000111111111111111 |
| -10 | 01110101 | 00000001111111111111111 |
| -11 | 01110100 | 00000011111111111111111 |
| -12 | 01110011 | 00000111111111111111111 |
| -13 | 01110010 | 00001111111111111111111 |
| ... | ... | ... |

  - use FP subtraction to get B in FP.

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- create FP value $v_l$=0 01111000 00000000001101001111001
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- $b$ = 0 01101101 10100111100100000000000
- this is the same as:

| c (9 bits) | a (9 bits) | b (18 bits) |
|---|---|---|
| 000000011 | 001111000 | 11010011110010000 |

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- Common-subexpression
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- Assembly
  - use a floating-point multiplier

# Enhanced reciprocal exponent handling

- compute reciprocal of denominator:
  - mantissa $M_d = 1 + y$, $y \in [0, 1)$
  - the exponent of the denominator $e_d^{biased} = e_d + bias$.
- the reciprocal:
  - mantissa $1/M_d \in (0.5, 1]$
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$$\begin{aligned} e_r^{biased} &= -e_d + bias \\ &= 2bias - e_d^{biased} \end{aligned}$$

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- normalization $\rightarrow$ exponent adjustment
  - let $n$ be true if need to normalize, or $1/M_d \in (0.5, 1)$.
  - $e_{rPostNorm}^{biased} = 2bias - e_d^{biased} - n$.
  - use bit manipulations to directly get $2bias - n$

$$\begin{aligned} 2bias - n &= 11111110 - n \\ &= 111111\widetilde{n}n \end{aligned}$$

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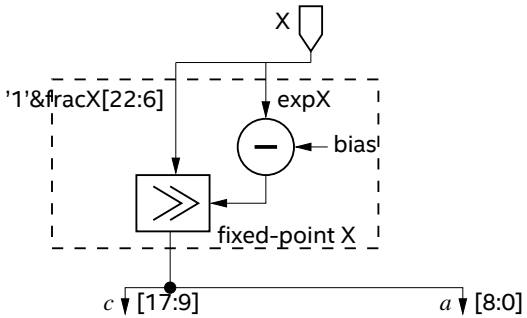

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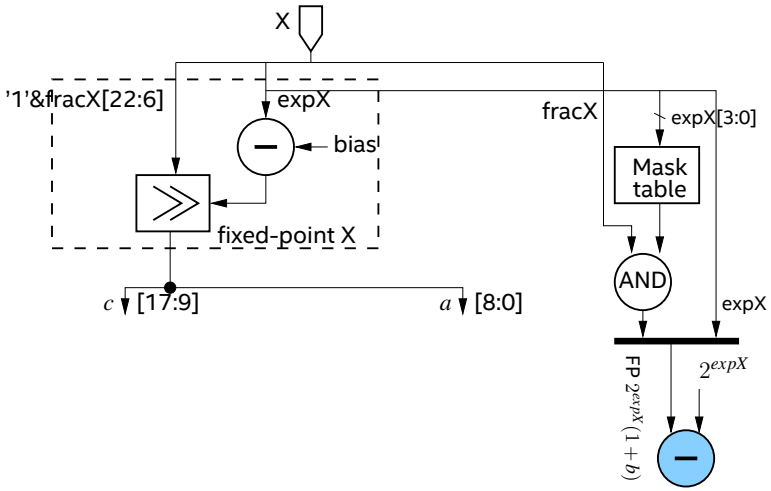

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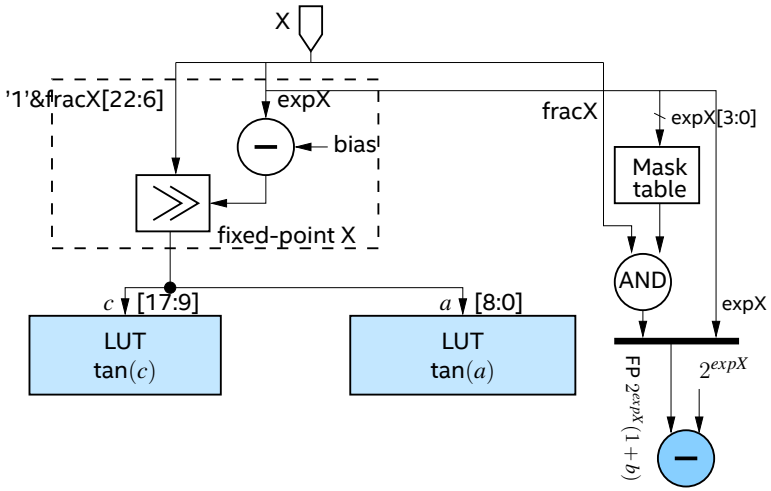

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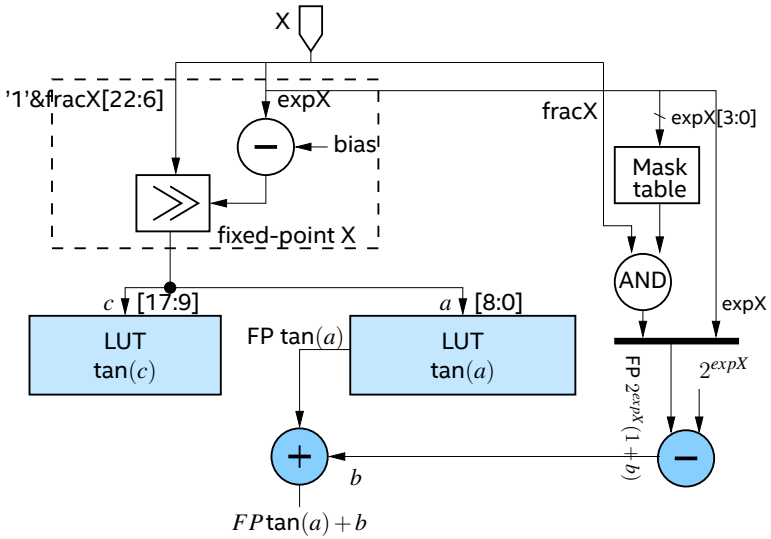

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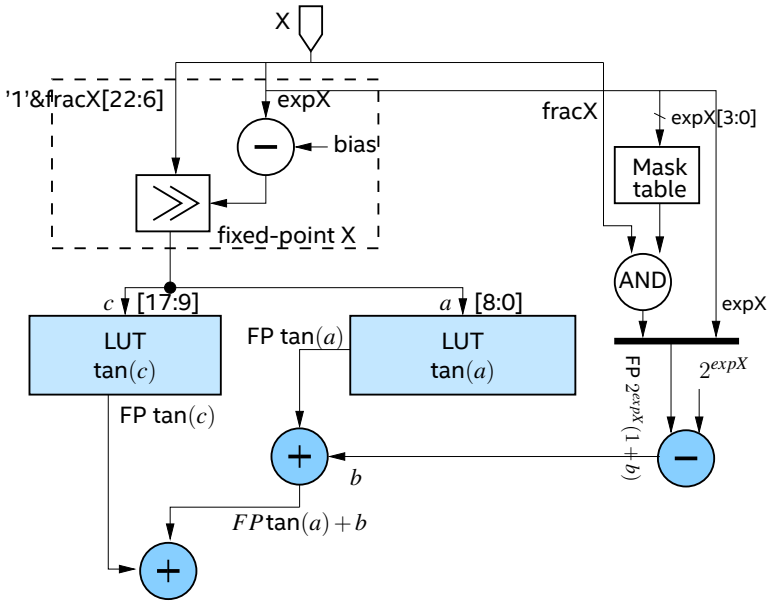

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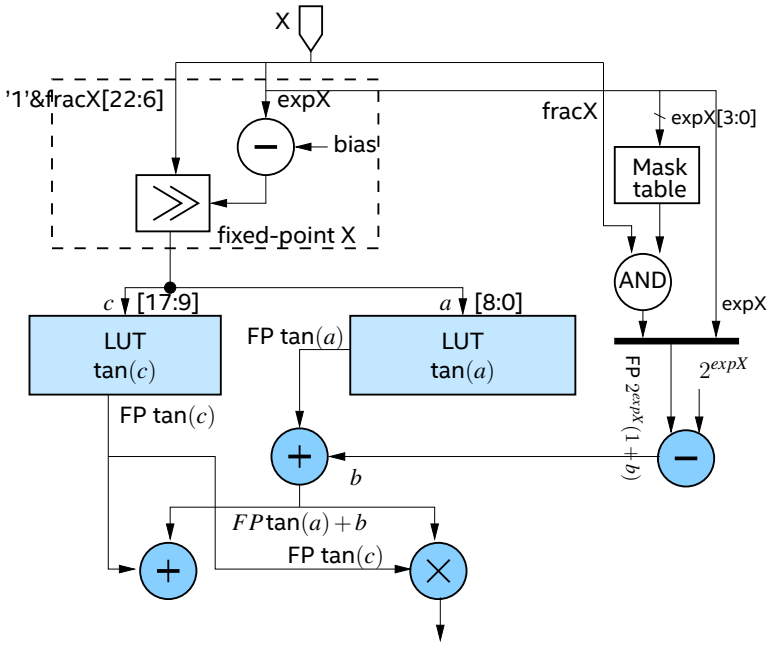

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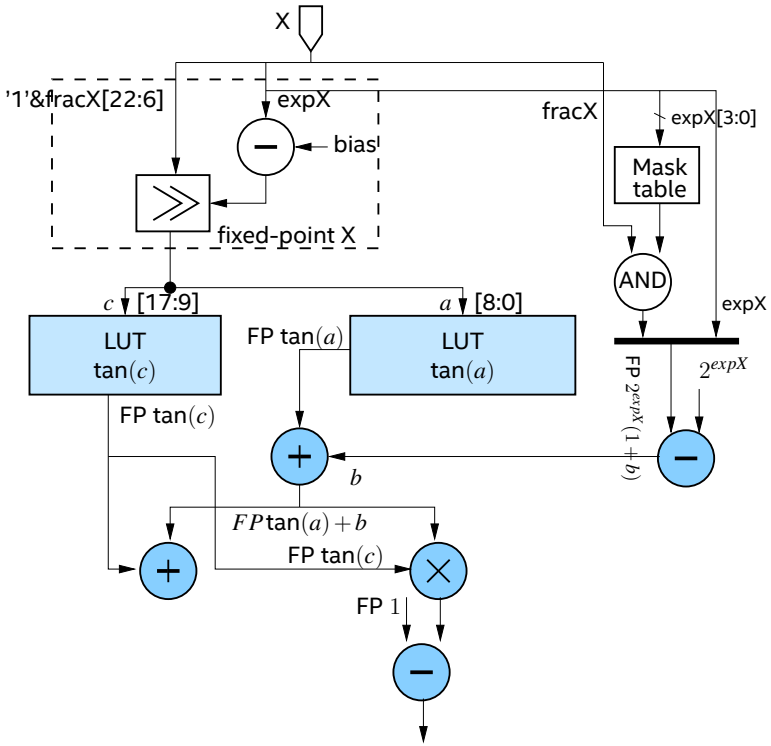

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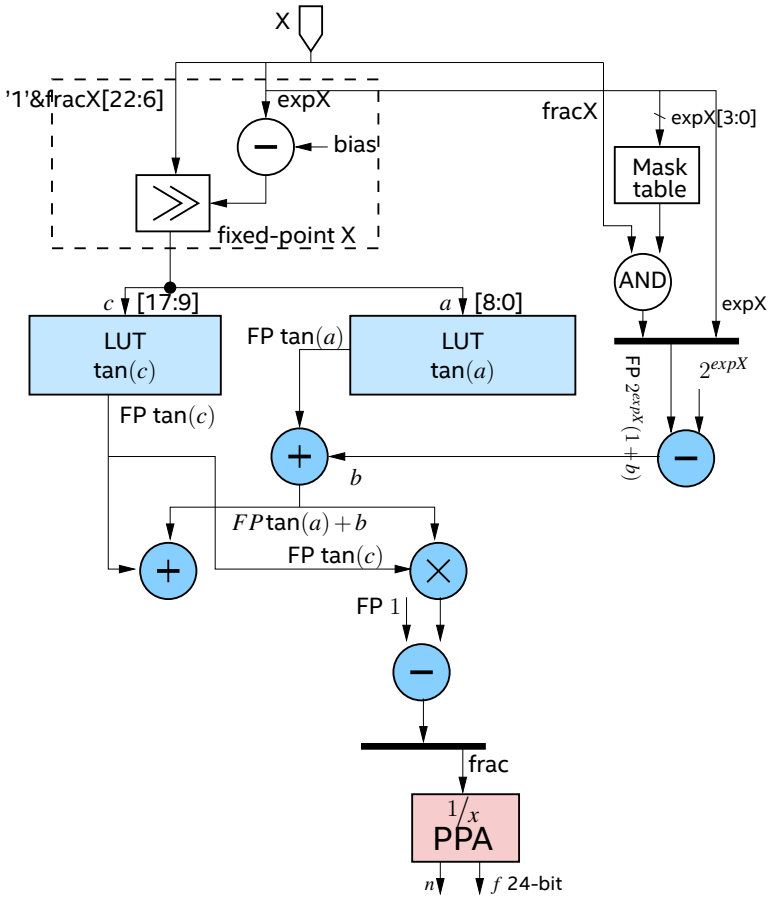

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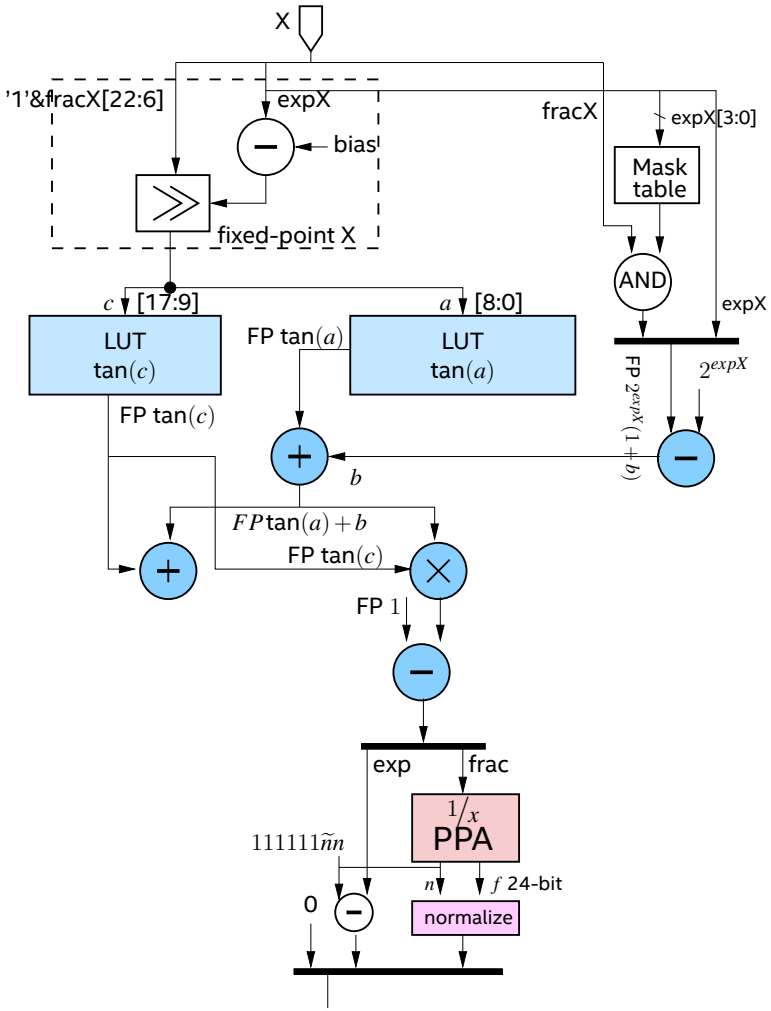

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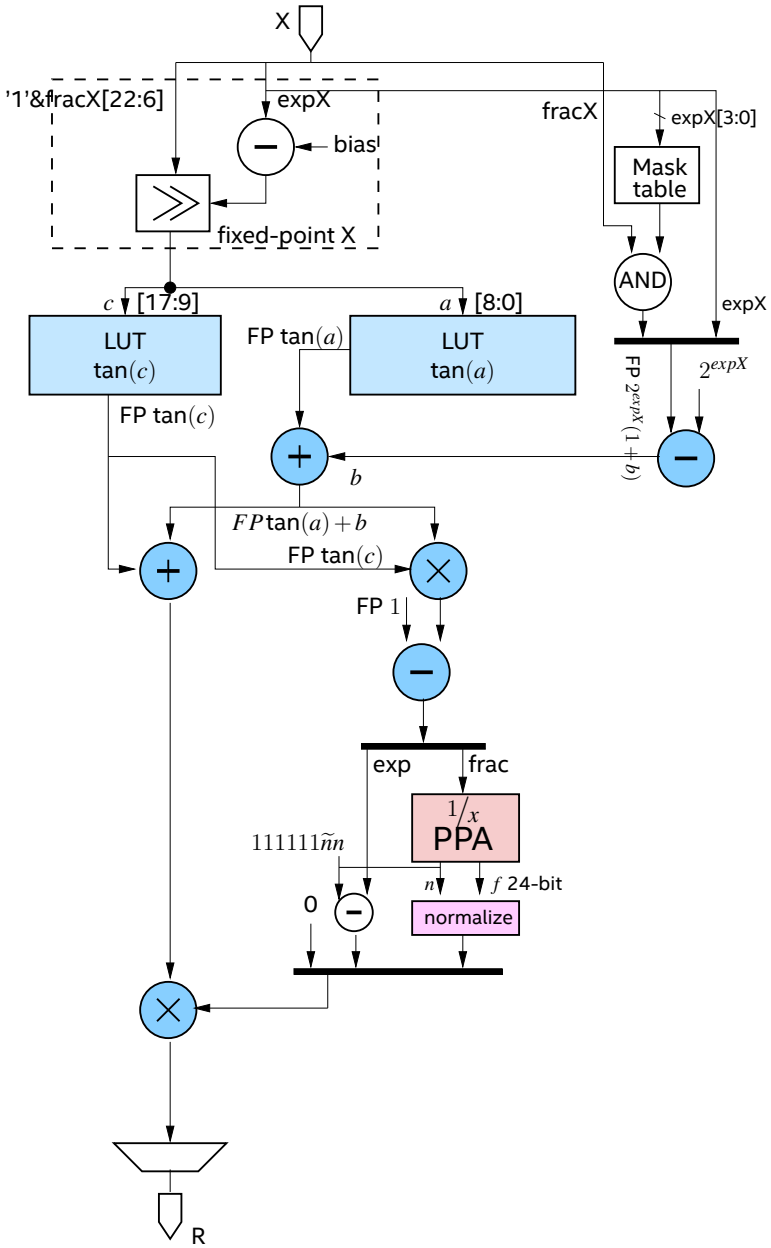

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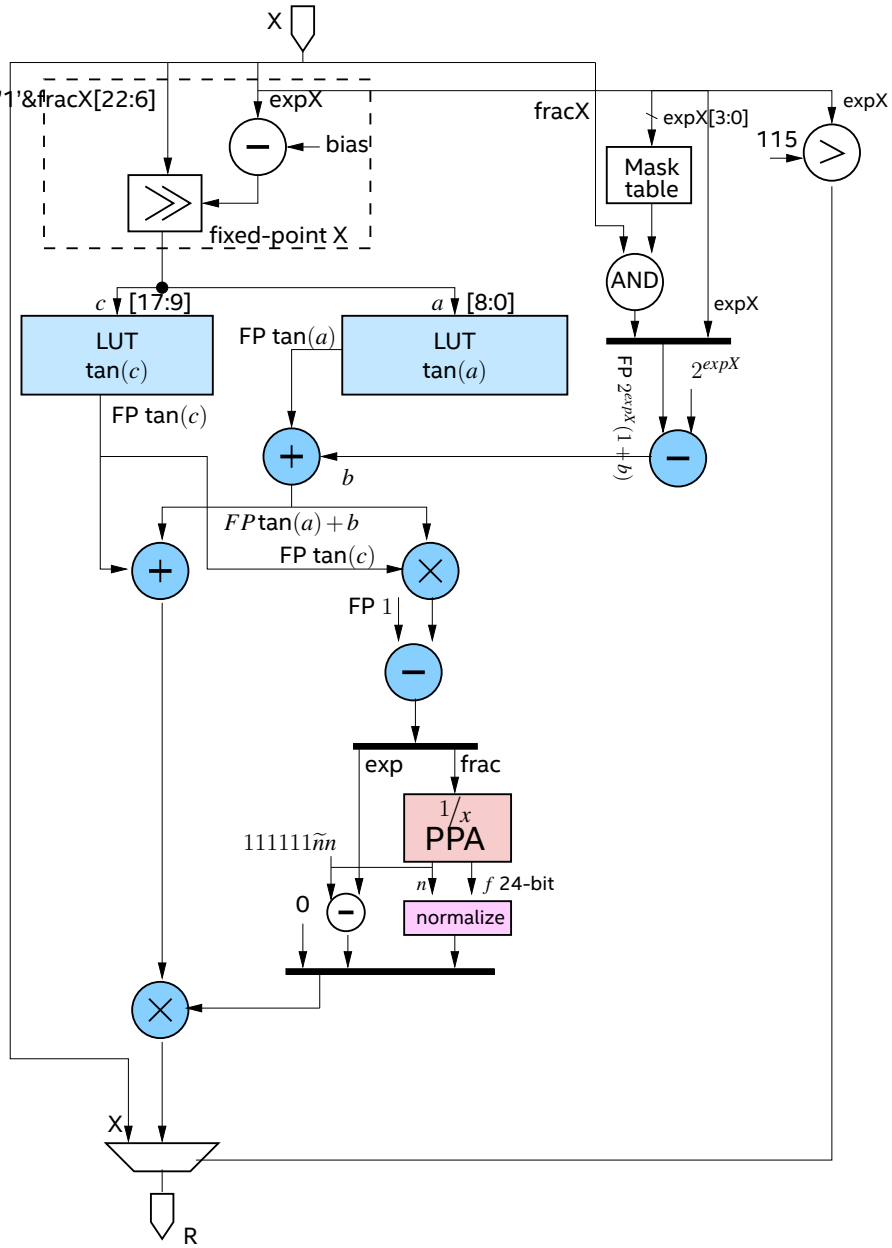

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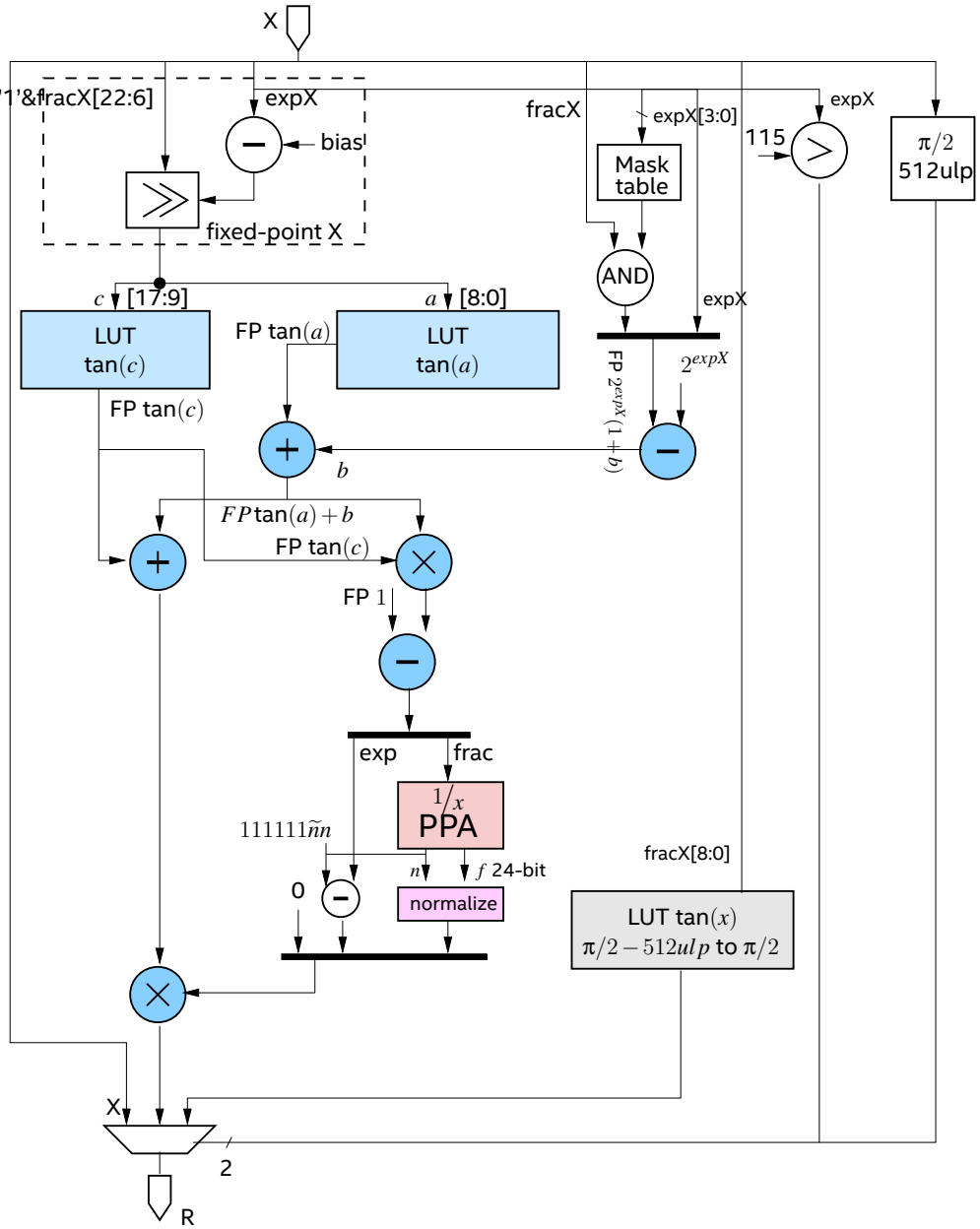
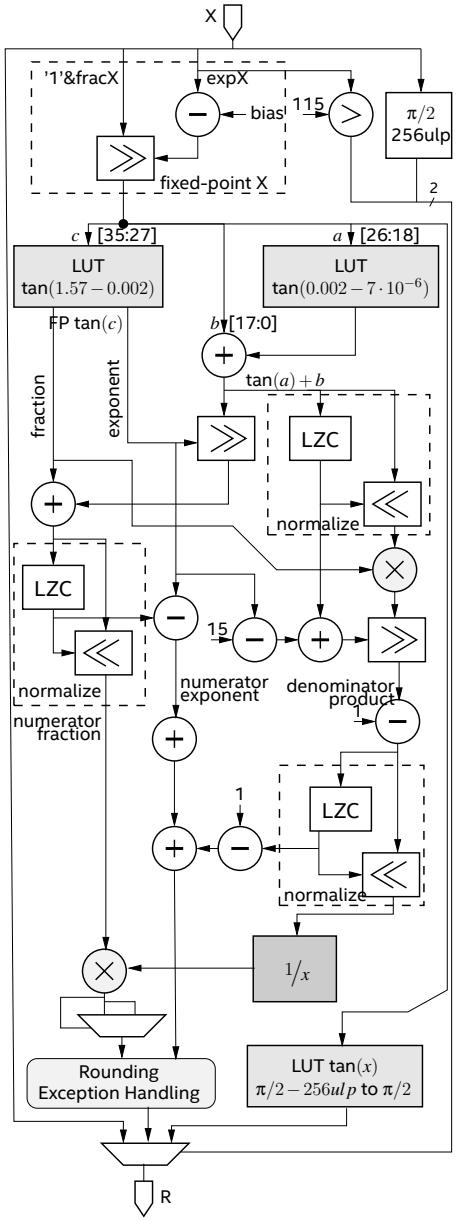
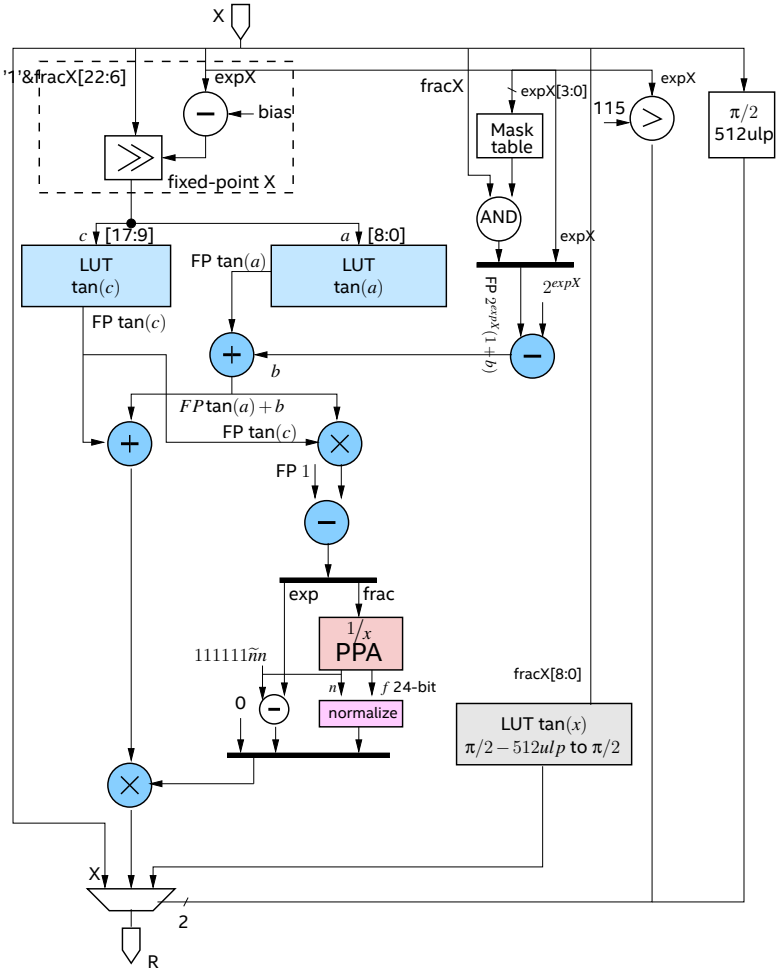


# Side-by-side comparison against non-HFP architecture



# Results

Table: Synthesis results for recent FPGA architectures

| Target | Architecture | Latency @ Freq. | Resources |
|---|---|---|---|
| Arria 10 | Proposed | 36 @ 520MHz | 8 DSPs, 6 M20K, 990ALMs |
| Stratix 10 | Proposed w/o HIPI | 53 @ 532MHz | 8 DSPs, 7 M20K, 1573ALMs |
| Stratix 10 | Proposed HIPI * | 53 @ 655MHz | 8 DSPs, 7 M20K, 1632ALMs |
| Arria 10 | Proposed FP | 32 @ 487MHz | 8 DSPs, 6 M20K, 393ALMs |
| Stratix 10 | Proposed FP w/o HIPI | 39 @ 573MHz | 8 DSPs, 6 M20K, 566ALMs |
| Stratix 10 | Proposed FP HIPI * | 39 @ 644MHz | 8 DSPs, 6 M20K, 572ALMs |

- results for both proposed architectures
- throughput of 1 operation / clock cycle
- largest Arria 10 472200 ALMs
  - Utilization of 0.23% for Proposed, 0.09% Proposed FP
- same Arria 10 1518 DSPs
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- HyperFlex architecture enhances Stratix 10 performance
- Stratix 10 ALMs $\times$ 2, DSPs $\times$ 3.8, M20Ks $\times$ 4.3

# Conclusion

- proposed fused-operator for single-precision tangent
- error analysis allows meeting OpenCL accuracy requirements
- proposed cores are fully pipelined, throughput 1 operation/cycle
- proposed cores require very little area
- DSP and Memory centric architectures allow reaching high frequencies
- Stratix 10 and Arria 10 Hard FP DSP block allows for an efficient implementation
- lower latency in high-frequency scenarios

# References


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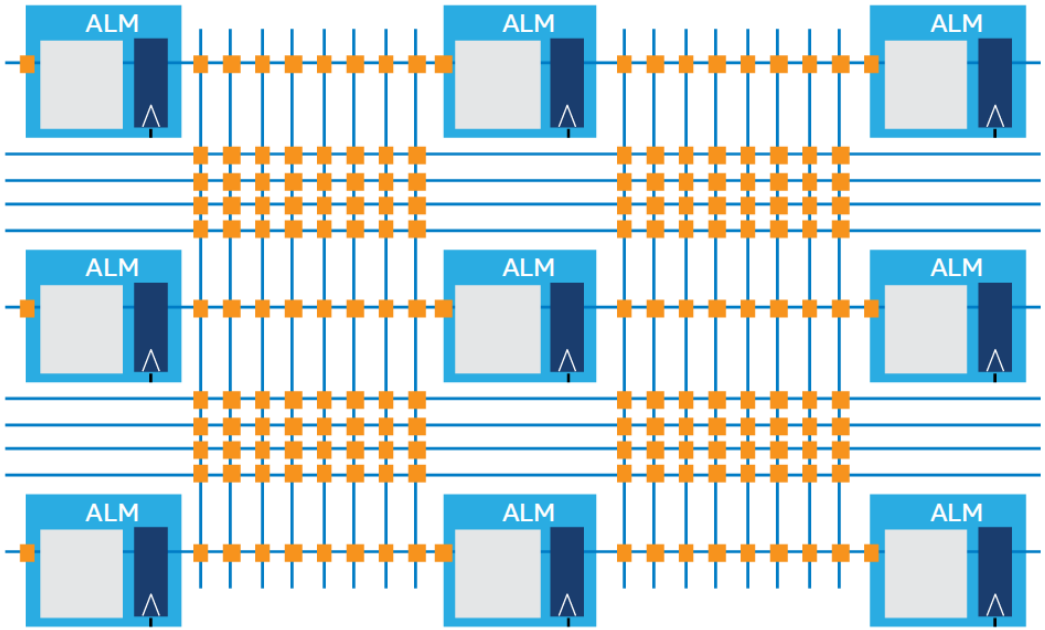
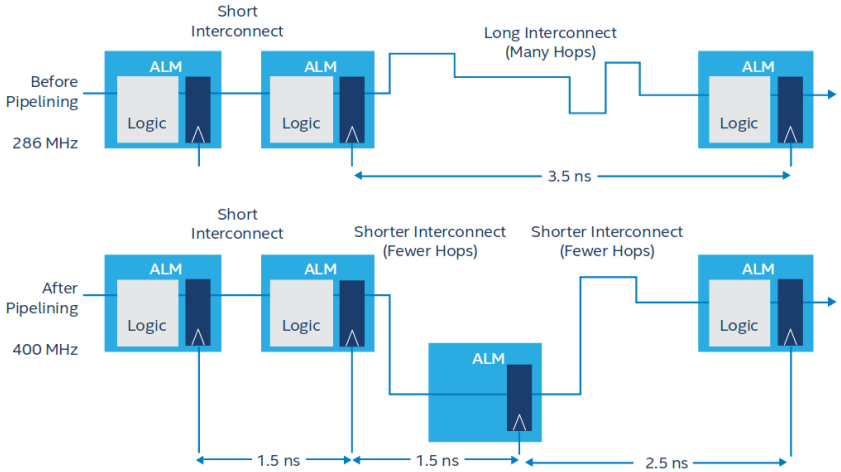
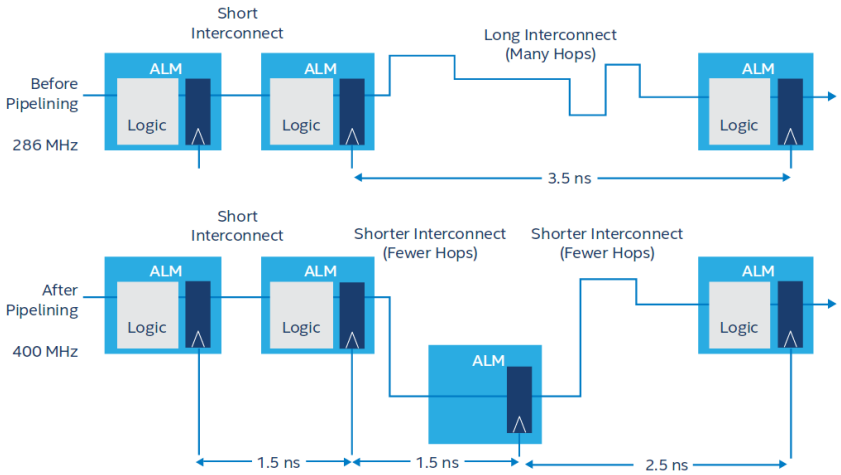
Figure: ”Registers Everywhere” HyperFlex Architecture



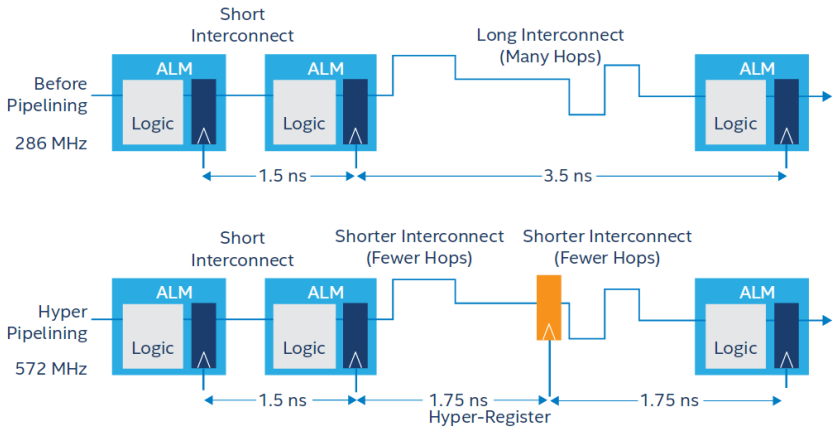
# Figure: Pipelining in Conventional FPGA Architectures



## Figure: Pipelining in Conventional FPGA Architectures




## Figure: Hyper-Pipelining in the HyperFlex Architecture

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